Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

In the Claims

1. (Currently Amended) A liquid crystal display comprising:

a liquid crystal panel assembly including a plurality of gate lines, a plurality of data lines which are insulated from and intersects the gate lines, and a plurality of pixels each of which is formed in an area defined by a data line of the data lines and a gate line of the gate lines and has a switching element connected to the gate line and the data line;

a gate driver for supplying gate voltages to the gate lines;

at least one data driver for supplying data voltages corresponding to image data to the data lines; and

a timing controller for comparing [[nth]] image data of an nth line applied from outside and ~~(n-1)th~~ image data of an (n-1)th line stored therein and selectively providing the [[nth]] image data of the nth line to the data driver depending on the comparison result, wherein the timing controller does not provide the [[nth]] image data of the nth line to the data driver when all bits of the [[nth]] image data of the nth line and the image data of the (n-1)th line ~~image data~~ are equal, and wherein the timing controller also does not provide the [[nth]] image data of the nth line to the data driver when all bits of the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line are complementary to each other.

2. (Currently Amended) The liquid crystal display of claim 1, wherein the timing controller generates an operation control signal based on the comparison result and provides the operation control signal to the data driver and the data driver is operated with a mode, based on the operation control signal, selected from a holding mode which provides data voltages corresponding to the stored ~~(n-1)th~~ image data of the (n-1)th line, an inverting mode which provides data voltages corresponding to the inverted ~~(n-1)th~~ image data of the (n-1)th line, and an updating mode which provides data voltages corresponding to the nth image data provided from the timing controller.

3. (Currently Amended) The liquid crystal display of claim 2, wherein the timing controller includes:

a first line memory for storing the [[nth]] image data of the nth line applied from outside;

a second line memory in which the (n-1)th image data applied in advance are stored; and

a control signal generator for generating [[an]] the operation control signal after comparing the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line, wherein[[; and]]

the control signal generator [[that]] generates:

[[an]] the operation control signal of a first status to let the data driver operate with the holding mode when all bits of the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line are equal to each other;

[[an]] the operation control signal of a second status to let the data driver operate with the inverting mode when all bits of the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line are complementary to each other; and

[[an]] the operation control signal of a third status to let the data driver operate with the updating mode when at least one bit of the [[nth]] image data of the nth line and at least one corresponding bit of the ~~(n-1)th~~ image data of the (n-1)th line are not equal or complementary to each other.

4. (Canceled)

5. (Currently Amended) The liquid crystal display of claim 3, wherein the timing controller generates [[an]] the operation control signal whose status changes by 1H period by comparing the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line during 1H period and the data driver holds, inverts, or updates the image data by 1H period.

6. (Currently Amended) The liquid crystal display of claim 3, wherein the timing controller generates [[an]] the operation control signal whose status changes as many times as the number of the data drivers by 1H period by comparing the [[nth]] image data for the nth line and

the ~~(n-1)th~~ image data for the (n-1)th line for each data driver during 1H period and the data driver holds, inverts, or updates the image data for each data driver.

7. (Currently Amended) The liquid crystal display of claim 3, wherein the timing controller generates [[an]] the operation control signal whose status changes as many times as the number of pixels of the line by 1H period by comparing the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line for each pixel during 1H period and the data driver holds, inverts, or updates the image data for each pixel.

8-9. (Canceled)

10. (Original) The liquid crystal display of claim 1, wherein the liquid crystal display has a COG (chip on glass) structure.

11. (Previously Presented) The liquid crystal display of claim 1, wherein the image data is transmitted to the data driver by RSDS (reduced swing differential signaling).

12. (Currently Amended) A driving method of a liquid crystal display, which includes a plurality of gate lines, a plurality of data lines which are insulated from and intersects the gate lines, and a plurality of pixels each of which is formed in an area defined by a data line of the data lines and a gate line of the gate lines and has a switching element connected to the gate line and the data line, the method comprising:

providing data voltages according to image data to the data line; and

making the data voltage be applied to the pixel by providing a gate voltage to the gate line,

wherein the provision of data voltages includes:

comparing ~~(n-1)th~~ image data of an (n-1)th line provided in advance and [[nth]] image data of an nth line being provided currently;

providing data voltages corresponding to the ~~(n-1)th~~ image data of the (n-1)th line to the data line when all bits of the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line are equal to each other;

inverting the ~~(n-1)th~~ image data of the (n-1)th line and providing data voltages corresponding thereto when all bits of the [[nth]] image data of the nth line and the [[(n-1)th]] image data of the (n-1)th line are complementary to each other; and

providing data voltages corresponding to the [[nth]] image data of the nth line to the data line when at least one bit of the [[nth]] image data of the nth line and at least one corresponding bit of the ~~(n-1)th~~ image data of the (n-1)th line are not equal or complementary to each other.

13. (Currently Amended) The system of claim 12, wherein the provision of data voltages compares the [[nth]] image data of the nth line and the [[(n-1)th]] image data of the (n-1)th line during 1H period.

14. (Currently Amended The method of claim 12, wherein the provision of data voltages compares the [[nth]] image data of the nth line and the [[(n-1)th]] image data of the (n-1)th line for each data driver of the liquid crystal display during 1H period.

15. (Currently Amended) The method of claim 12, wherein the provision of data voltages compares the [[nth]] image data of the nth line and the ~~(n-1)th~~ image data of the (n-1)th line for each pixel during 1H period.